REMARKS

Applicant has studied the Office Action dated December 13, 2005. It is submitted that the application is in condition for allowance. Claims 1-19 are pending. Reconsideration and allowance of the claims in view of the following remarks are respectfully requested.

As an initial matter, Applicant respectfully traverses the decision of the Examiner to make this Office Action final when all rejections in this Office Action are based on new grounds of rejection that were not stated in an earlier Office Action. In this Action, the Examiner rejected all of the claims under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) based on Liu et al. (U.S. Patent Application Publication No. 2004/0048468). Applicant respectfully points out that the Liu reference was not cited in any previous Office Action.

According to MPEP § 706.07(a): "Under present practice, second or any subsequent actions on the merits shall be final, except where the examiner introduces a new ground of rejection not necessitated by amendment of the application by applicant, whether or not the prior art is already of record." In the previous Office Action dated April 18, 2005, the Examiner rejected all of the claims under 35 U.S.C. §102(b) and 35 U.S.C. §103(a) based on Tamura et al. (U.S. Patent No. 5,877,095).

In the previously-filed Amendment, Applicant did not switch from one subject matter to another or resort to any subterfuge to keep the application pending. See MPEP § 706.07. The Liu reference was introduced in this Office Action by the Examiner to show anticipation and obviousness of the present invention. Thus, the Examiner has introduced a new ground of rejection not necessitated by amendment of the application by applicant. It is therefore respectfully submitted that the "final" status of the present Office Action is premature and should be withdrawn, and that the attached "Provisional RCE" should be disregarded.

If the Examiner does not withdraw the final status of the present Office Action, Applicant respectfully requests that the attached "Provisional RCE" be treated as a regular RCE, so that the finality of the present Office Action will be withdrawn and this Response entered and considered.

Turning to the patentability of the application, claims 1, 6-13, and 16-19 were rejected under 35 U.S.C. § 102(e) as being anticipated by Liu et al. (U.S. Patent Application Publication No. 2004/0048468). Claims 2-5, 12, 14, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. in view of Applicant's Admitted Prior Art ("AAPA"). These rejections are respectfully traversed.

The present application has a priority date of September 12, 2002 (i.e., the date the corresponding European patent application was filed). The Liu et al. reference cited by the Examiner was filed in the U.S. Patent and Trademark Office on September 10, 2002, which is only two days before the priority date of the present application. Attached is a copy of a patent proposal made by Applicant (along with an English translation of the relevant portion) that was prepared prior to September 10, 2002. This establishes that the invention claimed in the present application was conceived and reduced to writing in a WTO member country prior to September 10, 2002, so the invention claimed in the present application was invented prior to September 10, 2002. Liu was filed in the U.S. Patent and Trademark Office on September 10, 2002, which is after the invention claimed in the present application was invented. Therefore, Liu cannot properly be cited against the present application as a prior art reference in a rejection under 35 U.S.C. § 102(e) or 35 U.S.C. § 103(a).

Further, Applicant submits that, without the Liu reference, the AAPA fails to render the invention recited in the pending claims obvious under 35 U.S.C. § 103(a). Therefore, it is respectfully submitted that the rejections of claims 1-19 under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a) should be withdrawn.

Applicant has examined the reference cited by the Examiner as pertinent but not relied upon. It is believed that this reference neither discloses nor makes obvious the invention recited in the present claims. In view of the foregoing, it is respectfully submitted that the application and the claims are in condition for allowance. Reexamination and reconsideration of the application are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is invited to call the undersigned attorney at (561) 989-9811 should the Examiner believe a telephone interview would advance the prosecution of the application.

Respectfully submitted,

Date: June 13, 2006

By: _____

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Registration No. 40,917
Attorney for Applicant

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11 LUG. 2002
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Ns. Rif.: **02-AG-029**/RR-cs
EG

Agrate, 08/07/2002

Oggetto: Deposito di una domanda di brevetto a nome **STMicroelectronics Srl**

Inventori:
PIVIDORI Luca

Vi preghiamo di depositare, utilizzando la documentazione allegata, una domanda di Brevetto Europeo per una invenzione relativa a

PROTEZIONE DELLO STRATO DI PREMETAL PER LA DEFINIZIONE DI CONTATTI DA <0.21 um IN DISPOSITIVI DI MEMORIA NON VOLATILE

Sarebbe auspicabile che il deposito avvenisse entro il

31/8/02

in quanto esiste possibilita' di divulgazione dell'invenzione.

Gli stati da designare nella domanda sono Italia, Francia, Inghilterra, Germania e la lingua da utilizzare e' l'inglese.

Per ulteriori informazioni tecniche vogliate mettervi in contatto con gli inventori, presso i laboratori.

Con l'occasione, Vi porgiamo i nostri migliori saluti.

STMicroelectronics S.r.l.

cc: inventori

PATENT PROPOSAL 02-AG-029

*** CONFIDENTIAL ***

Descriptive Title of Invention:

PROTEZIONE DELLO STRATO DI PROTEZIONE PER LA AFFINIZIONE DI CONTATTI DA 0.2 µm IN DISPOSITIVI DI MEMORIA NON VOLATILE

Inventor(s):

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Tel: _____ Fax: _____

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Group: _____ Division: _____ Cost-Center: _____ CID: _____
Tel: _____ Fax: _____

4) First Name: _____ Family Name: _____
Private Address: _____
Employer: ST ☐ Corimme ☐ Site: _____
Other ☐ _____ Address: _____
Group _____ Division: _____ Cost-Center _____ CID: _____
Tel: _____ Fax: _____

STMicroelectronics

COMPANY RESTRICTED

Agrate, 10 January, 2002

From: Luca Pividori to: Ufficio Brevetti Agrate

-Proposta di brevetto-

Protezione dello strato di premetal per la definizione di contatti da <0.21µm in dispositivi di memoria non volatile.

Descrizione del problema

L'idea che costituisce questo brevetto permette di ovviare a 2 inconvenienti che si verificano nel modulo di processo che serve per la definizione del contatti in processi da 0.15μm o inferiori (ma cio` non toglie che si possa anche implementare in tecnologie piu` rilassate e quindi meno critiche).

Il metodo di seguito illustrato risulta particolarmente semplice ed e` di facile individuazione tramite una semplice analisi con sezione SEM in una qualunque zona del wafer, dato che i contatti vengono realizzati generalmente ovunque, sia nelle zone di matrice, sia nelle zone di circuiteria).

Arte nota

L'arte nota è costituita, in generale da tutti gli step di processo che sono utilizzati dagli addetti ai lavori per realizzare le strutture necesarie per definire zone di matrice e di circuiteria per un dispositivo di memoria flash.

Una volta realizzate le aree attive per la circuiteria e per la matrice di memoria del dispositivo flash si procede con gli step di processo che rappresentano sempre l'arte nota per produrre tali dispositivi:

1) crescita di un ossido attivo (tunnel)
2) deposizione e definizione del polysilicio che costituisce la floating gate (poly1) solo in matrice e suo eliminazione dalla circuiteria.
3) deposizione del dielettrico interpoly (comunemente ONO)
4) Tramite una maschera detta maschera MATRIX, si procede all'attacco (generalmente in dry) degli strati deposti di ossido interpoly (generalmente ONO) e del polisilicio della floating gate delle celle di memoria.
5) crescita di uno o piu` ossidi attivi di gate.
6) deposizione di un secondo strato di polisilicio
7) definizione delle celle della matrice mediante esposizione della maschera dell'autoallineato
8) definizione delle gates dei transistori mediante esposizione della maschera della circuiteria.

In seguito si procede con la formazione dello strato nel quale dovranno essere generati i contatti:

9) deposizione di uno strato di ossido, generalmente da HDP con uno spessore compreso tra 500Å-2500Å oppure di nitruro (nel caso in cui si utilizzi un processo per la formazione di contatti detti 'borderless')
10) deposizione di uno strato di BPSG, generalmente da SACVD, con concentrazione del tipo 2:9 utile specialmente per le richieste dei dispositivi di memoria flash.
11) reflow termico con RTA dello strato di BPSG deposto.
12) planarizzazione dello strato di premetal (USG+BPSG) ad esempio mediante tecnologia CMP.
A questo punto, secondo l'arte nota viene esposta la maschera dei contatti che prevede, per le maschere di tipo DUV, che vengano deposti dalla macchina litografia due strati sovrapposti di BARC e di resist. Tali strati sono necessari per permettere la definizione corretta dei

contatti secondo le specifiche dimensionali richieste dal prodotto, evitando anche la contaminazione del resist DUV da parte dello strato drogato di BPSG.

Processo proposto

L'idea che costituisce l'invenzione di questo brevetto e` quella di procedere nel seguente modo:

Dopo il punto 12), invece di esporre subito la maschera contatti, si deve deporre uno strato di nitruro UV trasparente da HDP, con uno spessore compreso tra 200Å 500Å (punto 5 nei disegni degli spaccati di processo).
La funzione di tale strato e` quella di:

a) evitare il contatto diretto del BARC+resist con il BPSG, anche in caso di prolungato stazionamento dei wafer con BARC+resist deposto e prima della loro lavorazione. In tale modo si evita la formazione di una difettosita` dello strato di BPSG, denominata 'corrosione' che rende impossibile la definizione dei contatti e provoca quindi una perdita di resa durante il testing del dispositivo (Fig.1).
b) Evitare la formazione di contatti denominati 'a doppio bordo', come da Fig.2 che sono critici quando la dimesioni dei contatti e` dell'ordine di grandezza dei 0.2 $\mu$m o minori e la distanza contact-to-contact e` dell'ordine di grandezza di 0.5μm.

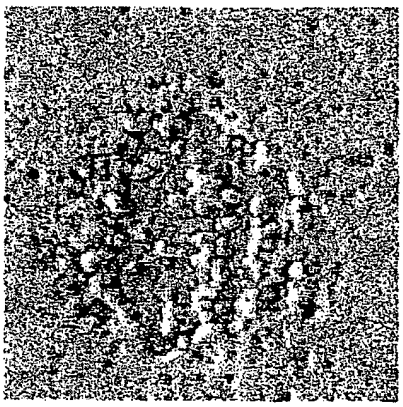


FIG.1

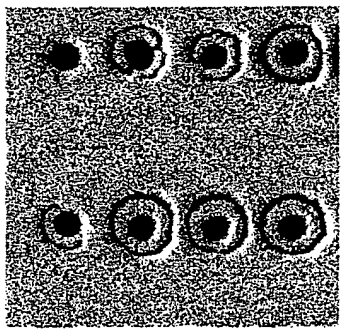


FIG.2

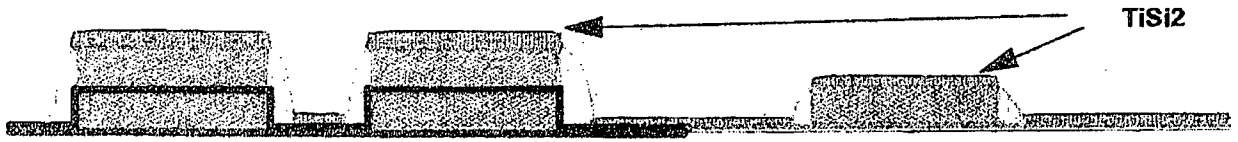
Lo strato deposto deve essere di un materiale che permetta di ottenere una selettivita` alta con il BPSG durante l'attacco dei contatti, in modo tale che, una volta che il resist ha ceduto (o e` stato consumato) svolga esso stesso la funzione di stopping layer superiore (cioe` al di sopra dello strato di BPSG) rispetto alla chimica dell'attacco. A questo proposito potrebbe essere vantaggioso che lo strato deposto sia un nitruro UV trasparente che presenta alta selettivita` con il BPSG e non inficia le performance affidabilistiche della cella di memoria, in particolare se la cella e` di tipo flash.

Uno volta deposto lo strato di protezione oggetto di questa proposta di brevetto, si procede con le normali operazioni di esposizione della maschera contatti e del suo attacco (punto 6 nelgi spaccati di processo allegati). Ovviamente la chimica dell'attacco sara` stata modificata in modo tale da attaccare correttamente nei primi step lo strato protettivo supplmentare, procedendo in maniera standard con la chimica di attacco ossido una volta giunti sul BPSG.

L'utilizzo di tale tecnica e` immediatamente identificabile, poiche` lo strato protettivo non e` previsto che venga rimosso dalla superficie del BPSG.

ARRAY CIRCUITRY **CONFIDENTIAL**

1



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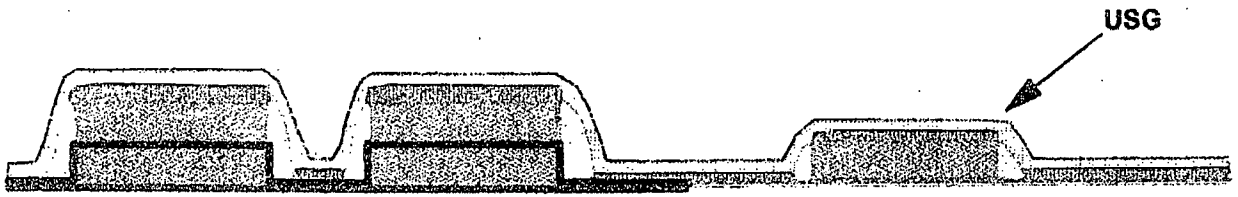

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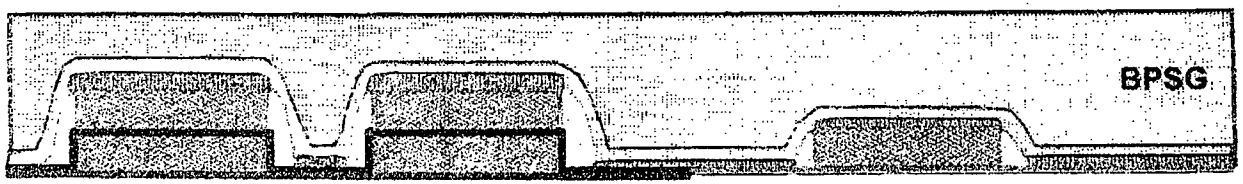
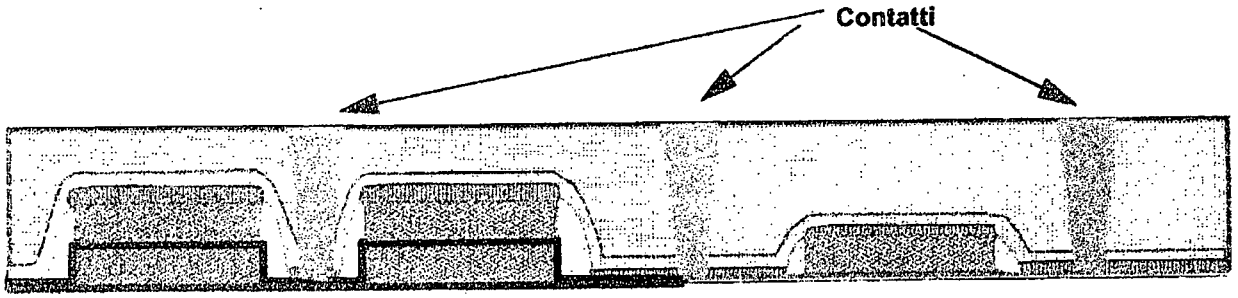


Luca Pividori - Central R&D - R2 Operations Device Flash Group

ARRAY CIRCUITRY **CONFIDENTIAL**

4



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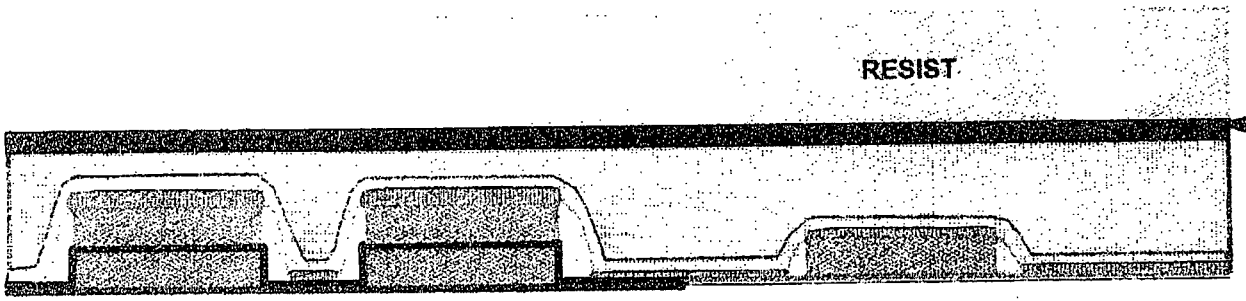

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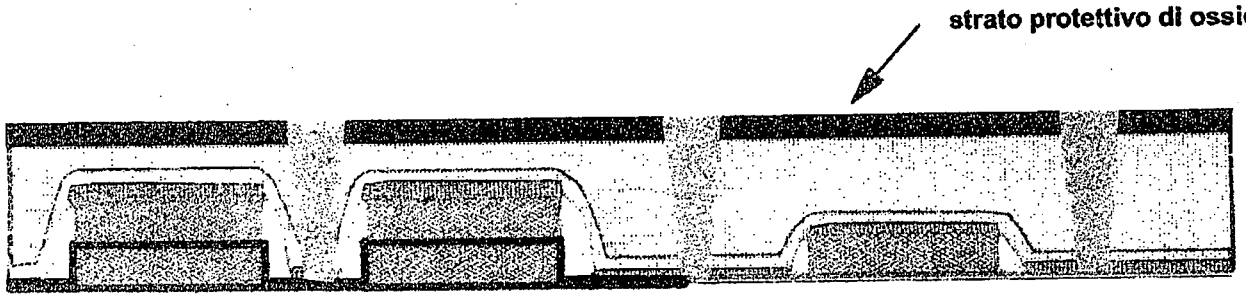

Page 1 of the document is a letter dated July 8, 2002.

This is its English translation:

"Our ref.: ***02-AG-029/RR*** *Agrate, 8 July 2002*

Subject: Filing of a patent application in the name of
STMicroelectronics S.r.l.

Inventor:

PIVIDORI Luca

We ask you to file, by using the annexed document, an European patent application for an invention related to:

PROTECTION OF A PRE-METAL LAYER FOR DEFINING CONTACTS LESS THAN 0.21um IN NON VOLATILE MEMORY DEVICES.

It would be desirable that the application is filed within

31 August 2002

because there is a possibility of disclosure of the invention.

The States to designate in the application are Italy, France, Great Britain, Germany and the language to use is the English.

For further technical information please contact the inventors, at the laboratories.

With the occasion, we give you our best greetings.

STMicroelectronics S.r.l.

copy to: inventors"

The second page of the document is already in English except for the descriptive title of the invention which is:

PROTECTION OF A PRE-METAL LAYER FOR DEFINING CONTACTS LESS THAN 0.21um IN NON VOLATILE MEMORY DEVICES.

This page comprises the name and the address of the inventor.

Pividori Luca
Via S. Pertini 18/H
24035 CURNO (BG)- Italy

./.

The translation in English of the document from the third page to the sixth page is:

Agrate, January 10, 2002

From: Luca Pividori *to: Patent Office Agrate*

-Patent proposal-

PROTECTION OF A PRE-METAL LAYER FOR DEFINING CONTACTS LESS THAN 0.21um IN NON VOLATILE MEMORY DEVICES.

Problem description:

The idea that constitutes this patent allows to solve two drawbacks which occur in the process for defining contacts in 0.15um or lower processes (however this idea can be implemented in less critical technologies)

The method which is herein described results simpler and it is easy to locate by means of an analysis with the SEM section in any region of the wafer because the contacts are formed everywhere both in the matrix regions and in the circuit regions.

State of the art:

The state of the art typically comprises all the steps of process which are used by the authorized personnel to form the structures necessary to define the matrix regions or the circuit regions of a flash memory device.

Once the active areas of the circuitry and of the matrix memory of the flash device are formed the process steps are effected which represent the state of the art to produce these devices:

1) Growth of an active oxide (tunnel);

2) Deposition and definition of a polysilicon layer that constitutes the floating gate (poly1) only in the active matrix and its elimination from the circuits;

3) Deposition of a dielectric interpoly layer (typically ONO);

4) Through a mask, said MATRIX mask, the attack (generally in dry) of the deposed layers of oxide interpoly (typically ONO) and of the polysilicon of the floating gate memory cells it is

effected;

5) Growth of one or more layers of gate active oxides;

6) Deposition of a second layer of polysilicon;

7) Definition of the matrix cells through exposure of the auto-alignment mask;

8) Definition of the transistors gates through exposure of the circuit mask.

Subsequently the formation of the layer in which should be generated the contacts is effected.

9) Deposition of an oxide layer typically from HDP process with a thickness among 500Å-2500Å, or of nitride (in the case in which for the formation of said contacts a process called borderless is used),

10) Deposition of a layer of BPSG, generally through a SACVD process, with concentration of the type 2:9 useful especially for memory flash devices.

11) Thermal treatment with RTA of the deposed BPSG layer.

12) Planarization of the pre-metal layer (USG+BPSG) for instance through CMP technology.

At this point, according to the known art the contact mask is exposed, which foresees the deposition from the lithographic machine of two overlapped layers of BARC and of resist, for the masks of the DUV type. Such layers are necessary to allow the correct definition of the contacts according to the dimensional specifications required by the product, by preventing even the contamination of the resist DUV from the doped layer of BPSG.

Proposed process:

The idea that constitutes the invention of this patent is that of proceeds in the following way:

After the phase 12), instead of immediately exposing the contact mask, a transparent UV nitride layer is deposed through a HDP process, with a thickness from 200Å to 500Å (indicated by the reference 5 in the drawings relative to the process).

The function of this layer is:

a) avoiding the direct contact of the BARC+resist with the BPSG, also in case of prolonged rest of the wafers with BARC+resist already deposed and before their working. In such a way the defectiveness formation called "corrosion" of the BPSG layer is avoided, which makes impossible the contact definition and therefore provokes a yield loss during the device testing

(Fig. 1).

b) avoiding the formation of contacts called "with double edge", as disclosed in Fig. 2, that are critical when the contact dimension is of the order of the 0.2 um or smaller than that and the distance between the contacts is of the order of 0.5um.

The deposed layer must be of a material that allows of getting a high selectivity with the BPSG during the contact attack, so that, once the resist is worn out (or it has been consumed) it develops the same function of upper barrier layer (that is above the BPSG layer) in comparison to the attack chemistry. To this purpose it could be advantageous that the deposed layer is for instance a transparent UV nitride that has high selectivity with the BPSG and does not prevent the reliability performances of the memory cell, particularly if the cell is of flash type.

Once the barrier layer has been deposed according to the patent proposal, the normal operations of mask exposure of the contact and its attack is effectuated (indicated by the reference 6 in the drawings relative to the process). Obviously the contact attack chemistry will be modified in order to correctly attach the additional protective layer in the first steps by proceeding in a standard way with the chemistry of the oxide etch once it is arrived on the BPSG.

The use of such a technology is immediately identifiable because the protective layer must be left on the surface of the BPSG.